CLAIMS

What is claimed is:

1. A method of fabricating a depletion drain-extended MOS transistor, comprising:

forming a first well of a first conductivity type in a substrate;

forming a second well of a second conductivity type in the substrate, the first and second conductivity types being opposite, wherein portions of the first and second wells overlap in a compensated channel region of the substrate;

forming a drain of the first conductivity type in a portion of the first well;

forming a source of the first conductivity type in a portion of the second well;

forming a thick dielectric extending laterally from a first end adjacent the drain to a second opposite end in the first well, the thick dielectric extending into the first well of the substrate;

forming a thin dielectric over the substrate, the thin dielectric extending from the second end of the thick dielectric in the first well to the source in the second well, a portion of the thin dielectric extending over the compensated channel region of the substrate; and

forming a conductive gate contact structure extending over the thin dielectric and over a portion of the thick dielectric.

2. The method of claim 1, further comprising providing dopants of the second conductivity type in an adjust region of the first well in the substrate proximate the second end of the thick dielectric.

3. The method of claim 2, wherein the first well has a concentration of dopants of the first conductivity type less than or equal to a first concentration value proximate the second end of the thick dielectric, and wherein the adjust region has a concentration of dopants of the second conductivity type at a second concentration value in the adjust region, the second concentration value being less than the first concentration value.

4. The method of claim 2, wherein providing dopants of the second conductivity type in the adjust region comprises implanting dopants of the second conductivity type in the adjust region.

5. The method of claim 4, wherein implanting dopants of the second conductivity type in the adjust region comprises performing a Vt adjust implant using a Vt adjust mask that exposes the adjust region of the substrate.

6. The method of claim 4, wherein implanting dopants of the second conductivity type in the adjust region is done after forming the thick dielectric.

7. The method of claim 2, wherein forming the thick dielectric comprises performing a LOCOS process.

8. The method of claim 2, wherein forming the thick dielectric comprises performing an STI process.

9. The method of claim 2, wherein the first conductivity type is n-type and the second conductivity type is p-type.

10. The method of claim 2, wherein forming the first well comprises implanting dopants of the first conductivity type into a portion of the substrate using a first well mask exposing the compensated channel region, and wherein forming the second well comprises implanting dopants of the second conductivity type into a portion of the substrate using a second mask exposing the compensated channel region.

11. The method of claim 10, wherein dopants of the first conductivity type are implanted using the first mask at a first implantation dose, wherein dopants of the second conductivity type are implanted using the second mask at

a second implantation dose, and wherein the first dose is greater than or equal to the second dose.

12. The method of claim 11, wherein the first conductivity type is n-type and the second conductivity type is p-type.

13. A method of fabricating a depletion drain-extended MOS transistor, comprising:

forming a source and a drain in a substrate, the source and drain being of a first conductivity type;

forming a gate structure over a channel region of the substrate, the gate structure comprising:

a thick dielectric having a first end adjacent the drain and extending laterally toward the source to a second opposite end, the thick dielectric extending into the substrate;

a thin dielectric extending over the substrate from the second end of the thick dielectric to the source; and

a conductive gate contact structure extending over the thin dielectric and over a portion of the thick dielectric;

forming a compensated channel region extending below a portion of the thin dielectric in the substrate, the compensated channel region comprising dopants of the first and second conductivity types; and

forming an adjust region in the substrate proximate the second end of the thick dielectric, the adjust region comprising dopants of the second conductivity type.

14. The method of claim 13, wherein providing dopants of the second conductivity type in the adjust region comprises implanting dopants of the second conductivity type in the adjust region.

15. The method of claim 14, wherein implanting dopants of the second conductivity type in the adjust region comprises performing a Vt adjust implant using a Vt adjust mask that exposes the adjust region of the substrate.

16. The method of claim 13, wherein the first conductivity type is n-type and the second conductivity type is p-type.

17. The method of claim 13, wherein forming a compensated channel region comprises:

implanting dopants of the first conductivity type into a portion of the substrate using a first well mask exposing the compensated channel region; and

implanting dopants of the second conductivity type into a portion of the substrate using a second mask exposing the compensated channel region.

18. The method of claim 17, wherein dopants of the first conductivity type are implanted using the first mask at a first implantation dose, wherein dopants of the second conductivity type are implanted using the second mask at a second implantation dose, and wherein the first dose is greater than or equal to the second dose.

19. A depletion drain-extended MOS transistor, comprising:

a source and a drain of a first conductivity type formed in a substrate;

a gate structure disposed over a channel region of the substrate, the gate structure comprising:

a thick dielectric having a first end adjacent the drain and extending laterally toward the source to a second opposite end, the thick dielectric extending into the substrate;

a thin dielectric extending over the substrate from the second end of the thick dielectric to the source; and

a conductive gate contact structure extending over the thin dielectric and over a portion of the thick dielectric;

a compensated channel region in the channel region of the substrate extending below a portion of the thin dielectric, the compensated channel region comprising dopants of the first and second conductivity types; and

an adjust region in the substrate proximate the second end of the thick dielectric, the adjust region comprising dopants of the second conductivity type.

20. The transistor of claim 19, wherein the drain is formed in a first well of the first conductivity type in the substrate and the source is formed in a second well of a second opposite conductivity type in the substrate.

21. The transistor of claim 20, wherein portions of the first and second wells overlap in the compensated channel region.

22. The transistor of claim 20, wherein the first well comprises dopants of the first conductivity type at a first concentration, wherein the second well comprises dopants of the second conductivity type at a second concentration, and wherein the first concentration is greater than or equal to the second concentration.

23. The transistor of claim 22, wherein the first conductivity type is n-type and the second conductivity type is p-type.

24. The transistor of claim 19, wherein the first conductivity type is n-type and the second conductivity type is p-type.

25. The transistor of claim 19, wherein the thick dielectric comprises a field oxide extending into and above the substrate.

26. The transistor of claim 19, wherein the thick dielectric comprises a dielectric material formed in a trench extending into the substrate.